Claims

What is claimed is:

1. A circuit comprising:
a first supply voltage port;
a second supply voltage port;
a current mirror circuit comprising a first current mirror port and a second current mirror port, the second current mirror port for propagating an input current from the first supply voltage port to the second supply port through the current mirror circuit coupled therebetween, where the first current mirror port is for providing N times the input current; and,
a current ratioing circuit comprising a first portion disposed between the first current mirror port and the second supply voltage port and a second portion disposed between the first supply voltage port and the second supply voltage port, the second portion comprising a load current path, where the current ratioing circuit is for propagating M times N times the input current through the load current path.

2. A circuit according to claim 1 comprising a current sink coupled between the second supply voltage port and the second port for sinking the input current through the current mirror circuit from the second current mirror port to the second supply voltage port.

3. A circuit according to claim 1 wherein the first portion of the current ratioing circuit comprises a first bipolar transistor having a first base terminal and one of a first collector terminal and first emitter terminal coupled with the first current mirror port and the other of the first emitter terminal and the first collector terminal thereof coupled with the second supply voltage port.

4. A circuit according to claim 3 wherein the second portion of the current ratioing circuit comprises a second bipolar transistor having a second base terminal coupled with the first base terminal and one of a second collector terminal and second emitter terminal coupled to the load current path and the other of the second emitter terminal and the second collector terminal thereof coupled with the second supply voltage port, wherein the second bipolar transistor is M times larger than the first bipolar transistor.

5. A circuit according to claim 3 wherein the second portion of the current ratioing circuit comprises a plurality of second bipolar transistor having a plurality of second base terminals coupled with the first base terminal and one of a plurality of second collector terminals and a plurality of second emitter terminals coupled to the load current path and the other of the plurality of second emitter terminal and the plurality of second collector terminal thereof coupled with the second supply voltage port, wherein the plurality of second bipolar transistors disposed together in parallel are M times larger than the first bipolar transistor.

6. A circuit according to claim 4 comprising a current path disposed between the first supply voltage port and the coupled first and second base terminals for propagating current therein in response to the input current.

7. A circuit according to claim 6 wherein the current path comprises a third field effect transistor (FET) having a third gate terminal, a third drain terminal and a third source terminal disposed in series along the current path, the third gate terminal coupled with the second current mirror port for controlling propagation of current between the third source and drain terminals in dependence upon the input current.

8. A circuit according to claim 1 wherein the current mirror circuit comprises:
a second FET having a second gate terminal, a second drain terminal and a second source terminal, the second source and second drain terminals disposed in series between the first supply voltage port and the second current mirror port.

9. A circuit according to claim 8 wherein the current mirror circuit comprises:
a first FET having a first gate terminal, a first drain terminal and a first source terminal, the first source and first drain terminals disposed in series between the first supply voltage port and the first current mirror port with one of the first drain and first source terminals coupled with the first gate terminal,
wherein the first FET is N times wider than the second FET.

10. A circuit according to claim 9 wherein the first FET is a PFET and the second FET is a PFET.

11. A circuit according to claim 2 comprising a second current source coupled to the first and second base terminals of the first and second bipolar transistors for providing an offset current thereto.

12. A circuit according to claim 11 wherein, in use of the circuit, a potential difference is realized between the second collector and second emitter terminals of the second bipolar transistor of approximately 300-400mV in response to the offset current.

13. A circuit according to claim 7 comprising a loop stabilization circuit comprising a first capacitor disposed between the third source and third gate terminals of the third FET; and,
a second resistor disposed between the third drain terminal of the third FET and coupled to a node formed between the first and second base terminals of the first and second bipolar transistors.

14. A circuit according to claim 13 comprising third and fourth resistors disposed between the first base terminal and the node and the second base terminal and the node, respectively.

15. A circuit according to claim 11 comprising a RF input port formed at the second base terminal of the second bipolar transistor for receiving of a RF input signal.

16. A circuit according to claim 7 wherein the load current path comprises a differential amplification stage disposed in series first supply voltage port and one of the second collector and second emitter terminals of the second bipolar transistor.

17. A circuit according to claim 16 wherein the differential amplification stage comprises:
first and second bias ports coupled to one of the third drain and third source terminals of the third FET;
a differential bias port coupled to one of the second collector and second emitter terminals of the second bipolar transistor;
a first RF signal input port for receiving a first RF input signal; and,
a second RF signal input port for receiving of a second RF input signal, where the first and second RF signal input ports are for, in combination, receiving of a differential RF input signal.

18. A method comprising:
providing a current mirror circuit having a first mirror portion and a second mirror portion, the first portion for propagating N times more current than the second portion;
providing a current ratioing circuit having a first portion and second portion, the second portion for propagating M times more current than the first portion;
propagating of an input current through a second portion of the current mirror circuit;
mirroring of the input current in the first portion to provide N times the input current;
receiving of the N times the input current by the current ratioing circuit; and,
ratioing of the N times the input current so that N times the input current propagates through the first portion and M times N times the input current propagates through the second portion.

19. A method according to claim 18 comprising:
providing a first voltage supply port coupled with the current mirror circuit and the current ratioing circuit; and,
providing a controlled current flow path between the first voltage supply port and first and second portions of the current ratioing circuit.

20. A method according to claim 18 comprising:
providing a load coupled with the current ratioing circuit for propagating the and M times N times the input current through the load.